JOURNAL OF NORTHEASTERN UNIVERSITY
Volume 25 Issue 04, 2022 ISSN: 1005-3026 https://dbdxxb.cn/ Original Research Paper

DESIGN OF SRAM USING FINFET AND ITS PERFORMANCE ANALYSIS

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ABSTRACT
Due to the loss of channel control, there are several problems with CMOS. Another topic covered in this paper is the impact of FinFET Gate Material Variation on Performance Characteristics. An SRAM cell optimised with FinFET technology is another example. The leakage currents and power dissipation are reduced when MOSFET-based memory arrays are replaced with quasi-planar FinFETs. Stability and area of the SRAM cell are critical design considerations. Fin width and pitch are the primary considerations when it comes to cell optimization. A few of these difficulties include an increase in leakage currents, an increase in on current, and a broad shift in parameter values. FinFET-based SRAM cell optimization was also shown. Fin width and pitch are the primary factors to consider while optimising a cell. High power consumption and an increase in leakage current afflict CMOS-based SRAMs, both of which have a detrimental effect on their performance. The static noise margin affects the cell's stability. A double-gate n-FinFET is the subject of this paper's modelling and simulation.
Keywords: SRAM, FINFET, Mosfet, performance, CMOS, IC, Chips, Memory, Power

INTRODUCTION
Standard SRAM cells are commonly used in memory systems because they meet strict performance criteria and are extremely simple to write or read. Two cross-coupled inverters create a latch in a 6T SRAM cell, which stores 1-bit of data and makes use of two transistors for reading and writing. The bit-lines, also known as input/output ports on the cell, are connected to the cell's internal nodes through a word-line that activates an access transistor. The precise size of transistors is critical to the stability of read and write operations. [1] Two cross-coupled inverters in a 6T SRAM cell drive bit lines high and low, respectively, during read operations, improving SRAM bandwidth compared to DRAM. CMOS, FinFET, and/or CNTFET devices can be used to create 6T-SRAM cells at appropriate technology nodes. Burn-in is the most essential screening method because it exposes package circuits to high voltages and temperatures at the same time. [2]
Voltage or temperature stress can also be given to circuits at the water level, before individual circuits are packed, to screen for flaws. Since early failures are often caused by the same faults

Submitted: 24/11/2022 **Accepted**: 09/12/2022

that cause yield (or time-zero) failures, yield improvement operations can lead to better early failure rates. In the steady-state regime, these same methods are beneficial in decreasing defects-related failures. [3] To be sure, circuit materials and transistor design are intrinsically prone to wear-out failures and steady-state electromechanical resistance (SER). This is why wear-out failure rates should be reduced throughout the technology development phase. For each mechanism, miniature test constructions may be designed to focus on certain materials and architectures, allowing extensive characterisation to be carried out for each mechanism.[4]

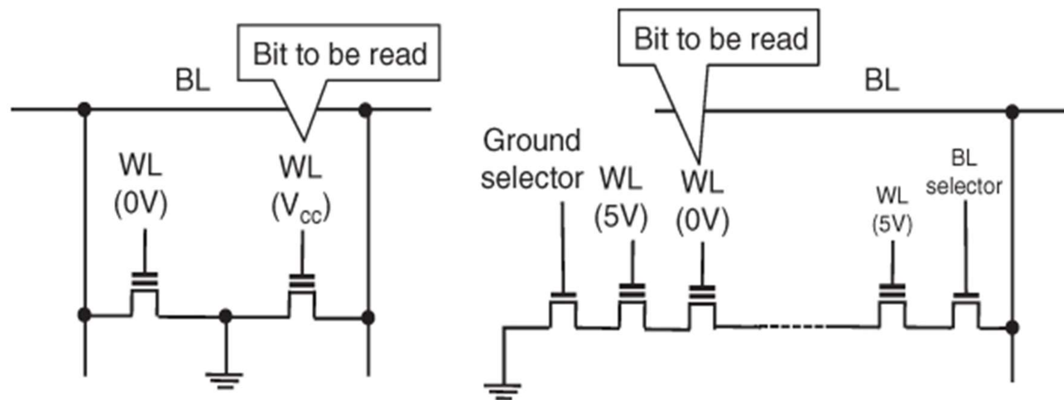

Figure 1 Gate circuit design for SRAM

Single-crystal gallium arsenide may be grown from this. Data may be stored in sequential logic circuits, which is why they are often referred to as memory elements. A D-latch and an FF, two classic sequential logic circuits, are shown here in simplified form. When the gate is open, the D-latch stores the input in an SRAM. The D-output latch's merely travels downstream from the D-latch.[5] Two latches make up the system: a master and a slave latch. The master latch detects an up-edge of a clock to maintain input data, but the data is not propagated to the slave latch. The second edge of the same clock pulse opens the slave latch gate once the inverted clock signal has reached it. After passing through two gates in the FF, the data appears at the FF's output. U. Mushtaq (2019) [6] Due to the significant increase in power dissipation in sub-micrometre area of operation, there arises a necessity to create low power circuits. The continuous scaling of CMOS logic circuits is not straight forward in the sense that when CMOS devices are scaled below 16nm, short channel effects are evident. The design of memory is of significant significance as there arises parameter fluctuations in CMOS SRAM cells when constructed below 16nm. Traditional SRAM cells can be replaced with FinFETs to overcome this problem. The design of a 7nm 6T FinFET SRAM cell utilising the ASAP7 PDK and Cadence virtuoso tool is given in this work. There are further considerations for things like power dissipation and noise margins that are examined. In compared to CMOS SRAM cells, the simulation results revealed that FinFET SRAM cell design may be very efficient. B. G. Kumar (2019) [7] Given current conditions, the VLSI industry has expanded tremendously while enforcing ever-tighter restrictions on crucial parameters like power, area, and speed. High-speed, low-power applications are urgently needed, as is the efficiency of such applications. The most popular memory cell for storing data until the power supply is turned

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on is the Static Random-Access Memory [SRAM] cell. The SRAM cell's power and delay limits are addressed in this study. The Adiabatic Logic method and FinFET technology are used to fulfil the restrictions. Compared to typical CMOS designs, FinFET based devices are more efficient with quicker switching rates and better power delay products. Utilizing previously saved energy, Adiabatic logic contributes to further reductions in electrical consumption. In order to minimise power consumption and latency, several adiabatic logics are applied to SRAM cells created with 18nm FinFETs in this article.

METHODOLOGY

FET switches with higher threshold voltage Vth between power supply and low Vth SRAM cell transistor are used to disconnect power supply and FET switches with higher threshold voltage Vth are used to disconnect ground from low Vth SRAM cell to minimise standby power. High speed and low switching power dissipation are possible when low Vth transistors are used in the active state. Sub-threshold leakage current is reduced when high Vth sleep transistors are turned off during sleep mode, resulting in a dissociation of the low Vth transistor from the supply voltage and ground. Concerns to the MTCMOS approach include the necessity for extra fabrication processes to achieve greater voltages and the fact that data cannot be retrieved by storage circuits based on this technique. SRAM cell implementation utilising MTCMOS technology.

A silicon fin with low doping Oxide contacts between source and drain gate regions is strongly doped in polysilicon (SiO2) Field Effects Based on Multi-FIN Structure of a Transistor It is possible to employ FINFET Double Gate (DG) devices in a number of novel methods, both digital and analogue, in the design of electronic circuits. The source and drain terminals of two transistors are connected in series to form a parallel transistor pair. Short channel effects and leakage current can be better controlled in Double-Gate (DG) FINFETS because the second gate is added opposite to the standard gate. The modes of FINFETs are identified as short gate (SG) mode, independent gate (IG) mode, low-power (LP) mode, and hybrid (IG/LP) mode. DG FINFET's front and back gates may be independently controlled in order to increase performance and minimise power consumption in this way. The use of independent gate control in non-critical pathways allows the parallelization of transistors.

The properties of FINFET based transistors are important to understand the model parameters. Current and voltage across a transistor are used to describe the basic properties of a FINFET. Comparison of the Vt roll-on between FINFET and Planer based FETs the high-k/Metal gate stack threshold voltage may be controlled through FINFET. FINFET does not need to suppress the SCE by using planar FETs with dual capping layers and high channel dopant concentrations to achieve a similar Vt at a long gate length. As a result, FINFETs may be more easily integrated into the whole process. Temperature and voltage are the primary determinants of the drain-to-source current. As voltage or temperature rises, drain current drops, reducing mobility carrier and threshold voltage. In the future, it is projected that memories would take up the majority of space. As a result, scalability is made significantly more difficult and crucial. With FINFET, a gate's electrostatic control is improved thanks to many sides of the fin controlling

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it. Multi gate MOSFETs reduce short channel phenomena such subthreshold degradation, Vth roll of width length, and drain induced barrier lowering (DIBL)... SRAM cells based on FINFET technology are preferred over CMOS-based SRAM cells because they offer a shorter access time, lower power consumption, and lower leakage current. The reduced power consumption of FINFET based SRAM cells has made them increasingly common. The 6T SRAM cell structure based on FINFETs is distinct from that of a normal SRAM. The primary memory consists of two cross-coupled inverters, while the access transistors are based on FINFETs. In order for the access transistors to operate, they must be linked to the word line and the bit line (bl) and bar correspondingly.

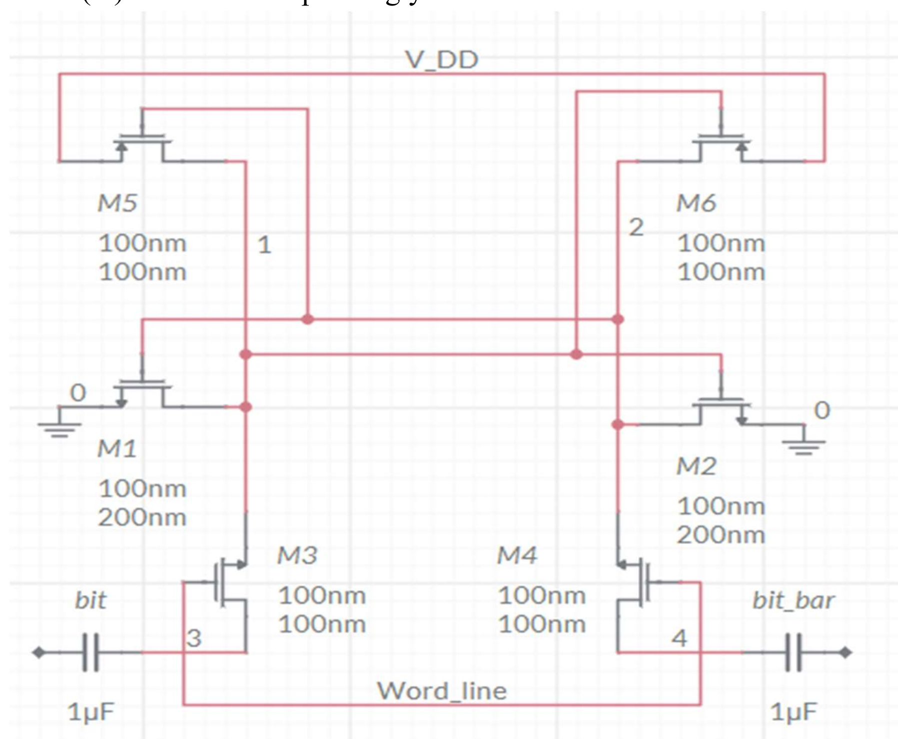

Figure 2 SRAM Circuit design

The access transistors must always be turned on while the memory element is being read or written to. Word line access transistors are activated during write and read operations, but are switched off under hold conditions. In order to use SRAM based on FinFETs, this cell has been designed. To put it another way, a lot of microelectronic frameworks are put on hold for long periods of time. The DC-DC converter's ability to enter or exit a low-power mode must be taken into account. Policy of entering low standby power when the system is idle may be implemented if the cost of transitioning to and from a standby mode is low enough. When implementing a power management strategy, we must take into account the predicted length of the standby state. To reduce the leakage currents in the STANDBY or ACTIVE model. A phase diagram can be used to explain the behaviour of a combination. It is possible for a substance to exist in a variety of states (solid, liquid, or gaseous). Two components, gallium and arsenic are shown on a phase diagram as a function of temperature. NOR and NAND are the two types of floating gate memories that may be used to read data. NOR and NAND floating gate memory

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use different circuitry. There is just one device connected to a BL (Bit Line) and ground when using NOR floating gate memory. To read data in a floating gate, the channel must be "ON" (state 1), which means there must be no electrons (state 1) in the floating gate for the current to pass between the BL and ground. The control gate's positive potential cancels out the negative potential of the floating gate, preventing the source-drain channel from opening when the floating gate is fully charged with electrons.

SLC floating gate memory has just two potential levels ('0' and '1'), dependent on the number of electrons in the floating gate, but MLC floating gate memory contains more than two states, often four charge states that yield two digits, '00,' '01, '10 and '11'. NAND floating gate memory employs a sequence of floating gates linked by a BL selector (transistor) and a ground selector at either end. All floating gates' control gates' potentials are kept high enough (5 V, for example) to turn their respective channels "ON," regardless of the potential of the floating gates, when data in one of the floating gates has to be read. A flow of current is only possible if the SLC floating gate being read is set to "1," else the data to be read is '0. IC production has been the driving force behind the expansion of the global electronic industry for the past half a century.

In the future, it is evident that ICs will continue to play a significant role: Moore's law dictates that additional advances in IC technology, either by improving performance and density with lower cost and power, or expanding system functionality, would allow ever more pervasive electronic systems. Reliability of circuits has always been a major challenge in IC development. As deterioration mechanisms are found during testing or in the field, it has become possible to ensure that ICs work as intended during the planned lifetime. The long-term failure rate of circuits as determined by accelerated testing measures, shows that the failure rate of circuits has decreased rapidly with technological advancement. Over the first 30 years of IC development, failure rates fell exponentially because to the combined efforts of technology development, manufacturing, circuit design and failure analysis specialists.

RESULT

A multiplexer circuit directs the relevant cell outputs to data registers in order to choose the bits. Each cell in the array is kept in two rows of eight columns each. For a 4Mb memory reduction, this design uses rows and columns both equal to 64. An 8Mb SRAM memory may be created using two of these memory slices. Data bits stored in a memory array may be modified (written) and retrieved using an R/W memory circuit known as the SRAM IC (reading). The CDS IC446 cadence IC design environment was used to create the SRAM IC. Using the AMI 0.6-micron process, we were able to create this design. In addition, there is no current discharge in the read route. Unlike 6T SRAM, 8T SRAM has a write driver instead of a pre-charging circuit. Bit line leakage is a minor leakage current that occurs when the read „1 operation is executed. One extra transistor is utilised in the read route to solve this issue.

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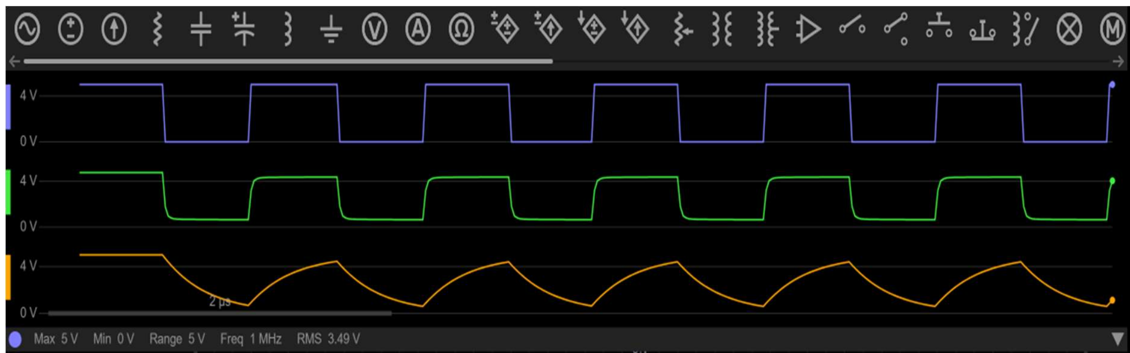

Figure 3 SRAM cell to reduce read power

The stacking effect refers to the reduction in bit line leakage that occurs as a result of the addition of another transistor. The RBL swing is decreased by using a 10T SRAM cell to reduce read power. If the last data written was "1" or "0," charge sharing is conducted between RBL and BLB or RBL and BL while reading "0." During the following cycle, the pre-charge circuit uses less power since the RBL is not drained correctly due of charge sharing. The bit line is pushed up to full swing voltage from a middle-voltage value. A write driver is used to reduce the amount of power needed to write. The data value determines whether the bit line is moved up or down by the write driver. Read "0" results in a passage of discharge current through the read route and M9 to BL, thus BL is somewhat charged. After writing "1," BL is driven to "1" using the write driver. After reading "0," you can reduce the power. A single bit of data may be stored in a 6T cell of the new 6T SRAM, which has six transistors. Because it takes a little amount of space, 6T SRAM is a popular choice, however it has certain stability difficulties. Two access transistors and two cross-coupled inverters are included. The cell has a word line (WL), a bit-line (BL), and a bit-line-bar (BLB) for correct functioning (BLB). A read/write operation can only be carried out with the access transistors enabled when WL=1. In the 6T FinFET SRAM, there are two inverters. The M1 and M2 transistors are used in the first inverter, while the M1 and M2 transistors are used in the second inverter. Access transistor M5 and M6 are available. Bit-line, world-line, and bit-line-bar are also available for read and write operations. SRAM FinFET of 6T The 6T FinFET SRAM A two-way inverter is included. Using M1 and M2 transistors, the first inverter is constructed. The second inverter is constructed using M1 and M2. M5 and M6 are the two transistors used for gaining access to the device.

Figure 4 SRAM stability and performance

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The bit-line, world-line, and bit-line-bar are also present for read and write operations. The 8-transistor SRAM (B) Additionally, 8T SRAM features two NMOS transistors, making it nearly identical to 6T SRAM. The stability of 6T SRAM was compromised by the inclusion of two transistors in 8T SRAM. Multimedia applications benefit from its inclusion. The read-bit-line (RBL) in 8T SRAM is pre-charged to full swing for read operations. Transistor M6 is switched on, and RBL is discharged to ground through transistors M5 and M6, assuming Q = 0. RBL's voltage drops are picked up by the sense amplifier. transistor M6 remains in the off state in read "1" and Q = "1". Double Gate with Independently Driven Entry: The two gates on the independent gate DG FinFET are maintained apart from each other. Multiple threshold voltages are possible since each gate biases itself individually. As a result, the overall number of transistors is reduced. Leakage current is minimised in the independent gate DG SRAM cell. As a result, the cell's stability and performance improve. The breadth of fins should be kept to a minimum. These inverters can be used to regulate individual pull-up transistors' alternative gates.

CONCLUSION

As CMOS and FINFET's performance is dependent on transistor density, SRAM-based memory systems have been selected as the best way to compare the two technologies. FinFET-based SRAM cell nodes outperformed 6T CMOS SRAM cells in the simulations when it came to static noise margin. CMOS based SRAM architecture has a higher read and write latency than FINFET. All structures have been subjected to transient analysis for standby, read, and write SRAM cell operations, and average power and latency have been calculated. Bulk CMOS-based SRAM versus FINFET-based SRAM has been compared to determine whether mode performs better in terms of leakage power, dynamic power, latency for writing and reading, and SNM for writing operations. Power Delay Product and Static Noise Margin performance metrics were compared to those of a 6T CMOS SRAM cell for the purpose of determining the differences. The thickness of the fin and the channel are observed to be the FINFET and CMOS design device parameters, respectively, from the study carried out in this research. Using nanoscale technologies, such as FinFET-based SRAM cells, this research examines the performance of these devices.

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